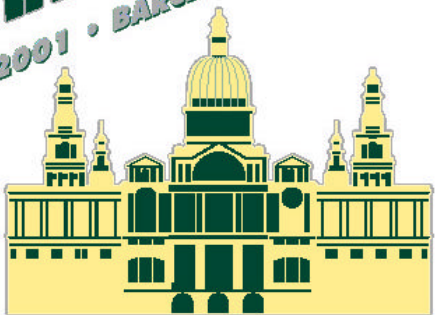


2001 INTERNATIONAL CONFERENCE ON  
**PARALLEL ARCHITECTURES  
AND  
COMPILATION TECHNIQUES**  
8-12 SEPTEMBER 2001 • BARCELONA, CATALUNYA, SPAIN



# Final Program

PACT01

## Final Program

### Saturday, September 8th

#### 08:00 – Workshops Registration

#### 08:30 – 19:00 EWOMP'01

European Workshop on OpenMP. Organizers: Eduard Ayguadé (Technical Univ. of Catalunya, Spain) and Tim Mattson (Intel Corporation, USA)

#### 08:30 – 13:30 WBT'01

Workshop on Binary Translation. Organizers: Erik Altman (IBM T.J. Watson Research Center, USA) and David Kaeli (Northeastern Univ., USA)

#### 09:00 – 13:00 MEDEA'01

Workshop on Memory Access Decoupled Architectures. Organizers: Roberto Giorgi (Univ. of Siena, Italy), Antonio Prete (Univ. of Pisa, Italy) and Jelica Protic (Univ. of Belgrade, Yugoslavia)

### Sunday, September 9th

#### 08:00 – Workshops and Tutorial Registration

#### 09:00 – 19:00 EWOMP'01

Continuation from previous day.

#### 08:55 – 18:20 COLP'01

Workshop on Compilers and Operating Systems for Low Power. Organizers: Luca Benini (Univ. di Bologna, Italy), Mahmut Kandemir (Penn State Univ., USA) and Jagannathan Ramanujam (Louisiana State Univ., USA)

#### 09:00 – 13:00 UCC'01

Workshop on Ubiquitous Computing and Communication. Organizers: Ulrike Lucke and Djamshid Tavangarian (Univ. of Rostock, Germany)

#### 09:00 – 17:00 Tutorial

"The Design and Implementation of the Jalapeño JVM". Michael Hind and Dick Atanasio (IBM Research).

#### 20:00 - Welcoming Reception

### Monday, September 10th

#### 08:00 – Conference Registration

#### 08:45 - Conference Opening

#### 09:00 - Keynote Address

"Influence of Technology Directions on System Architecture." Randall D. Isaac (VP Science and Technology, IBM Research).

#### 10:00 - Session 1: Simulation and Modeling

*Chair: Steve Keckler, Univ. of Texas - Austin*

"Basic Block Distribution Analysis to Find Periodic Behavior and Simulation Points in Applications." Tim Sherwood, Erez Perelman and Brad Calder, (Univ. of California, San Diego)

"Modeling Superscalar Processors via Statistical Simulation."

Sebastien Nussbaum and James Smith (Dept. of Electrical and Computer Engineering, Univ. of Wisconsin-Madison)

"Hybrid Analytical-Statistical Modeling for Efficiently Exploring Architecture and Workload Design Spaces." Lieven Eeckhout and Koen De Bosschere (Department of Electronics and Information Systems, Ghent Univ.)

#### 11:30 - Coffee Break

#### 12:00 - Session 2: Efficient Caches

*Chair: Brad Calder, Univ. of California San Diego*

"Filtering Techniques to Improve Trace-Cache Efficiency."

Roni Rosner, Avi Mendelson and Ronny Ronen (Israel Design Center, Intel)

"Reactive-Associative Caches."

Brannon Batson (Compaq) and T. Vijaykumar (Purdue Univ.)

"Adaptive Mode Control: A Static-Power-Efficient Cache Design."

Huiyang Zhou, Mark Toburen, Eric Rotenberg and Thomas Conte (North Carolina State Univ.)

#### 13:30 - Lunch Break (on your own)

#### 15:00 - Session 3: Specialized Instruction Sets

*Chair: Jim Dehnert, Transmeta*

"Implementation and Evaluation of the Complex Streamed Instruction Set."

Ben Juurlink (1), Dmitri Tchereassiz (2), Stamatis Vassiliadis (1), Harry Wijshoff (2). (1) Electrical Engineering Department, Delft Univ. of Technology. (2) Department of Computer Science, Leiden Univ.

"On the Efficiency of Reductions in micro-SIMD media extensions."

Jesus Corbal, Roger Espasa, and Mateo Valero (Computer Architecture Department, UPC)

#### 17:00 - Excursion to Montserrat and Reception at Cavas Vinery



<http://www.ac.upc.es/pact01>

## Tuesday, September 11th

### 09:00 - Keynote Address

"Electronics in the Internet Age. Justin Rattner (Intel Fellow, Director of Microprocessor Research Labs).

### 10:00 - Session 4: Prediction and Recovery

*Chair: Antonio Gonzalez, UPC*

"Boolean Formula-based Branch Prediction for Future Technologies."

Daniel Jimenez (1), Heather Hanson (2) and Calvin Lin (1), (1) Department of Computer Sciences, (2) Department of Electrical & Computer Engineering, The Univ. of Texas at Austin.

"Using Dataflow Based Context for Accurate Value Prediction."

Renju Thomas and Manoj Franklin (Univ. of Maryland)

"Recovery mechanism for latency misprediction".

Enric Moráncho, José María Llaberia and Angel Olive (Computer Architecture Department, UPC)

### 11:30 - Coffee Break

### 12:00 - Session 5: Memory Optimization

*Chair: Bilha Mendelson, IBM*

"A Cost Framework for Evaluating Integrated Restructuring Optimizations."

Bharat Chandramouli, John Carter, Wilson Hsieh and Sally McKee (Univ. of Utah)

"Compiling for the Impulse Memory Controller."

Xianglong Huang, Zhenlin Wang and Kathryn McKinley (Computer Science Dept., Univ. of Massachusetts)

"On the Stability of Temporal Data Reference Profiles." Trishul Chilimbi (Microsoft Research)

### 13:30 - Lunch Break (on your own)

### 15:00 - Session 6: Program Optimization

*Chair: Sally McKee, Univ. of Utah*

"Code Reordering and Speculation Support for Dynamic Optimization Systems."

Erik Nystrom, Ronald Barnes, Matthew Merten and Wen-mei Hwu (Univ. of Illinois)

"A Unified Modulo Scheduling and Register Allocation Technique for Clustered Processors."

Josep Codina, Jesus Sanchez and Antonio Gonzalez (Computer Architecture Department, UPC)

"Cache-Friendly Implementations of Transitive Closure."

Michael Penner and Viktor Prasanna (Univ. of Southern California)

### 16:30 - Coffee Break

### 17:00 - Session 7: Technology Implications

*Chair: Ali Hurson, Penn State Univ.*

"The Effect of Technology Scaling on CMP Throughput."

Jaehyuk Huh, Doug Burger and Stephen Keckler (Univ. of Texas at Austin)

"Area and System Clock Effects on SMT/CMP Processors."

James Burns (Intel) and Jean-Luc Gaudiot (Univ. Southern California)

### 18:15 - Work In Progress Session

Organizers: Martin Schulz (Technische Univ. München, Germany), Bruce Childers (Univ. of Pittsburgh, USA) and Sally McKee (Univ. of Utah, USA)

### 21:00 - Conference Banquet (Hilton Hotel)

## Wednesday, September 12th

### 09:00 - Keynote Address

"EV8: The Post-ultimate Alpha". Joel Emer (Intel Fellow, Intel Architecture Group Director).

### 10:00 - Session 8: Parallel Machines

*Chair: Kemal Ebcioglu, IBM*

"Limits on Speculative Module-level Parallelism in Imperative and Object-oriented Programs on CMP Platforms".

Fredrik Warg and Per Stenstrom (Chalmers Univ. of Technology)

"Compiler and Runtime Analysis for Efficient Communication in Data Intensive Applications".

Renato Ferreira (1), Gagan Agrawal (2) and Joel Saltz (1), (1) Univ. of Maryland, (2) Univ. of Delaware

"Architectural Support for Parallel Reductions in Scalable Shared-Memory Multiprocessors".

Maria Jesus Garzaran (1), Milos Prvulovic (2), Ye Zhang (2), Alin Jula (3), Hao Yu (3), Lawrence Rauchwerger (3) and Josep Torrellas (2), (1) Univ. de Zaragoza, Spain, (2) Univ. of Illinois at Urbana-Champaign, (3) Texas A&M Univ.

### 11:30 - Coffee Break

### 12:00 - Session 9: Data Prefetching

*Chair: Josep Torrellas, Univ. of Illinois at U-C*

"Optimizing Software Data Prefetches with Rotating Registers".

Gautam Doshi, Rakesh Krishnaiyer and Kalyan Muthukumar (Intel Corporation)

"Multi-Chain Prefetching: Effective Exploitation of Inter-Chain Memory Parallelism for Pointer-Chasing Codes". Nicholas Kohout (1), Seungryul Choi (2), Dongkeun Kim (3), Donald Yeung (3), (1) Intel Corp., (2) Department of Computer Science, (3) Department of Electrical and Computer Engineering, U. of Maryland at College Park

"Data Flow Analysis for Software Prefetching Linked Data Structures in Java".

Brendon Cahoon and Kathryn McKinley (Univ. of Massachusetts)

"Comparing and Combining Read Miss Clustering and Software Prefetching".

Vijay Pai (Rice Univ.) and Sarita Adve (Univ. of Illinois).

### 14:00 - Final Conference Address



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The Organizing Committee of PACT'01 gratefully acknowledges the support received from public institutions (Spanish Ministry of Education through the CICYT, Catalan Government through the CIRIT and Technical University of Catalunya UPC):



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Travel grants for students have been thanks to the generous support from Hewlett-Packard HPL, IBM Research, Intel and Microsoft Research:

