On mapping to multi/manycores

Jeronimo Castrillon
Chair for Compiler Construction (CCC)
TU Dresden, Germany

MULTIPROG – HiPEAC Conference
Stockholm, 24.01.2017
Mapping for dataflow programming models

- Dataflow: Successful abstraction across different domains

- Embedded
  - Resource and real-time constraints, heterogeneous platforms
  - Traditionally static models (reduce run-time overhead), but
  - Dynamic models needed: require profiling information
Mapping processes/actors & channels (well studied)

- Trace-based: Analyze “unrolled” executions to compute compile-time mappings

- Use meta-heuristics (popular: genetic algorithms)

- Need for
  - Better architecture models (standardization?)
  - Convergence of dataflow models (common IR?)
  - Compiler – run-time interaction
- Large applications with multiple constraints (e.g., communication standard)
- Memory re-used extremely important
- **ILP formulation** for temporal mapping of logical buffers to memories under bandwidth and memory size constraints
- Benchmark: 1ms LTE execution (1000 logical buffers) onto an 80-core machine

[Goens16]
Mapping data to data structures

- Changing graphs (e.g., in social networks)
- With some changes, better data-representations become more efficient
- Profiling and monitoring

(a) Degree distribution

(b) Connected components

[Schiller16] © Prof. J. Castrillon. HiPEAC, 2017
Mapping data to data structures

- Changing graphs (e.g., in social networks)
- With some changes, better data-representations become more efficient
- Profiling and monitoring

5.4x speedup (averaged over seven different graph metrics, Molecular dynamics benchmark)

(a) Degree distribution
(b) Connected components

© Prof. J. Castrillon. HiPEAC, 2017
More mapping to come

- HAEC project: wireless and optical system interconnect
- Map/configure communication architecture

- Cfaed Orchestration project on post-CMOS technologies
- Mapping data to heterogeneous memories (reliability, retention, ...)
- Map computation to truly heterogeneous resources
Summary

- Described several mapping problem formulations
  - Dataflow to heterogeneous multi-cores
  - Buffer lifetimes to interconnect and memories
  - Data to data structures

- Outlook: Interesting mapping problems coming up (e.g., in HAEC and cfaed)


